CLAIMS

1. A phase splitter for generating first and second complimentary output clock signals from an input clock signal, the phase splitter comprising:

an even number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the first output clock signal;

an odd number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the second output clock signal;

a first pair of transistors each of which is coupled between an output of one of the inverters in the even number of series connected inverters and respective first and second nodes; and

a second pair of transistors each of which is coupled between an output of one of the inverters in the odd number of series connected inverters and respective third and fourth nodes.

2. The phase splitter of claim 1 further comprising an inverter coupled between an output of an inverter that is N number of inverters from the input clock signal and an output of an inverter that is N+1 number of inverters from the input clock signal, where N comprises a positive integer.

3. The phase splitter of claim 2 wherein N comprises an odd positive integer.

4. The phase splitter of claim 1 wherein at least one transistor in each pair has a gate that is coupled to one of the first and second voltages.

5. The phase splitter of claim 4 wherein the transistors in each pair has a respective gate that is coupled to the first and second voltages, respectively.

6. The phase splitter of claim 1 wherein the first and second nodes comprises a common node.

7. The phase splitter of claim 6 wherein the first, second, third and fourth nodes comprises a common node.

8. The phase splitter of claim 7 wherein the common node comprises an output of one of the inverters that is an odd number of inverters from the input clock signal, and the inverter in each of the first and second branches having an output to which the respective first and second pairs of transistors are coupled comprise an odd number of inverters from the input clock signal.

9. The phase splitter of claim 1 wherein the transistor in each pair have a gate that is coupled to one of the inverters in one of the series of inverters.

10. The phase splitter of claim 9 wherein a first transistor in each pair is has a drain that is coupled to a supply voltage, and a second transistor in each pair is coupled to ground potential.

11. The phase splitter of claim 1 wherein the first and third nodes comprise a supply voltage, and the second and fourth nodes comprises a ground potential.

12. The phase splitter of claim 1 wherein the third and fourth reference nodes comprises a common node.

13. The phase splitter of claim 1 wherein the even number of series connected inverters comprises two inverters and the odd number of series connected inverters comprises three inverters.

14. The phase splitter of claim 13 wherein the first pair of transistors is coupled between an output of the third inverter in the odd number of series connected inverters and an output of the first inverter in the even number of series connected inverters, and the second pair of transistors is coupled between an output of the third inverter in the odd number of series connected inverters and an output of the first inverter in the odd number of series connected inverters.

15. The phase splitter of claim 1 wherein the even number of series connected inverters comprises 2 inverters and the odd number of series connected inverters comprises five inverters.

16. The phase splitter of claim 15 wherein the first pair of transistors is coupled between an output of the fifth inverter in the odd number of series connected inverters and an output of the first inverter in the even number of series connected inverters, and the second pair of transistors is coupled between an output of the third inverter in the odd number of series connected inverters and an output of the first inverter in the odd number of series connected inverters.

17. The phase splitter of claim 1, further comprising an electrical component loading the output of the first of the inverters in the odd numbered series and in the even numbered series, the electrical component being unconnected to any other portion of the phase splitter.

18. The phase splitter of claim 17, wherein each of the electrical component comprises a respective inverter.

19. The phase splitter of claim 1 wherein the transistors in the first and second pairs comprise diode-coupled transistors.

20. A phase splitter for generating first and second complimentary output clock signals from an input clock signal, the phase splitter comprising:

an even number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the first output clock signal;

an odd number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the second output clock signal; and

an inverter having an input coupled between an output of an inverter that is an odd number of inverters from the input clock signal and an output of an inverter in the that is an even number of inverters from the input clock signal.

21. The phase splitter of claim 20 further comprising an inverter having an input coupled between an output of an inverter that is N number of inverters from the input clock signal and an output of an inverter that is N+1 number of inverters from the input clock signal, where N comprises a positive integer.

22. The phase splitter of claim 21 wherein N comprises an odd positive integer.

23. The phase splitter of claim 20 wherein the even number of series connected inverters comprises 2 inverters and the odd number of series connected inverters comprises 3 inverters.

24. The phase splitter of claim 23 wherein the inverter has an input coupled to an output of the second inverter in the odd number of series connected inverters and an output coupled to an output of the first inverter in the even number of series connected inverters.

25. The phase splitter of claim 20 wherein the even number of series connected inverters comprises 2 inverters and the odd number of series connected inverters branch comprises 5 inverters.

26. The phase splitter of claim 20, further comprising an electrical component loading the output of the first of the inverters in the odd numbered series and in the even numbered series, the electrical component being unconnected to any other portion of the phase splitter.

27. The phase splitter of claim 26, wherein each of the electrical component comprises a respective inverter.

28. A phase splitter for generating first and second complimentary output clock signals from an input clock signal, the phase splitter comprising:

an even number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the first output clock signal;

an odd number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the second output clock signal; and

an electrical component loading the output of the first of the inverters in the odd series numbered and in the even numbered series, the electrical component being unconnected to any other portion of the phase splitter.

29. The phase splitter of claim 28, wherein each of the electrical component comprises a respective inverter.

30. A memory device, comprising:

an array of memory cells;

an address decoder adapted to receive an address and to specify a location in the array of memory cells corresponding thereto;

a read/write circuit coupling data to and from the specified location in the array of memory cells;

a control logic circuit receiving command signals and generating control signals corresponding thereto; and

a phase splitter coupled to the control logic circuit, the phase splitter being operable to receive an input clock signal and to apply first and second complimentary output clock signals corresponding thereto, the phase splitter comprising:

an even number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the first output clock signal;

an odd number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the second output clock signal;

a first pair of transistors each of which is coupled between an output of one of the inverters in the even number of series connected inverters and respective first and second nodes; and

a second pair of transistors each of which is coupled between an output of one of the inverters in the odd number of series connected inverters and respective third and fourth nodes.

31. The memory device of claim 30 further comprising an inverter having an input coupled between an output of an inverter in the even number of series connected inverters that is N number of inverters from the input clock signal and an output of an inverter in the odd number of series connected inverters that is N+1 number of inverters from the input clock signal, where N comprises a positive integer.

32. The memory device of claim 31 wherein N comprises an odd positive integer.

33. The memory device of claim 30 wherein at least one transistor in each pair has a gate that is coupled to one of the first and second voltages.

34. The memory device of claim 33 wherein the transistors in each pair has a respective gate that is coupled to the first and second voltages, respectively.

35. The memory device of claim 30 wherein the first and second nodes comprises a common node.

36. The memory device of claim 35 wherein the first, second, third and fourth nodes comprises a common node.

37. The memory device of claim 35 wherein the common node comprises an output of one of the inverters that is an odd number of inverters from the input clock signal, and the inverter having an output to which the respective first and second pairs of transistors are coupled comprise an odd number of inverters from the input clock signal.

38. The memory device of claim 30 wherein the transistor in each pair have a gate that is coupled to one of the inverters in one of the series of inverters.

39. The memory device of claim 38 wherein a first transistor in each pair is has a drain that is coupled to a supply voltage, and a second transistor in each pair is coupled to ground potential.

40. The memory device of claim 30 wherein the third and fourth reference nodes comprises a common node.

41. The phase splitter of claim 30 wherein the first and third nodes comprise a supply voltage, and the second and fourth nodes comprises a ground potential.

42. The memory device of claim 30 wherein the even number of series connected inverters comprises two inverters and the odd number of series connected inverters comprises three inverters.

43. The memory device of claim 42 wherein the first pair of transistors is coupled between an output of the third inverter in the odd number of series connected inverters and an output of the first inverter in the even number of series connected inverters, and the second pair of transistors is coupled between an output of the third inverter in the odd number of series connected inverters and an output of the first inverter in the odd number of series connected inverters.

44. The memory device of claim 30 wherein the even number of series connected inverters comprises 2 inverters and the odd number of series connected inverters comprises five inverters.

45. The memory device of claim 44 wherein the first pair of transistors is coupled between an output of the fifth inverter in the odd number of series connected inverters and an output of the first inverter in the even number of series connected inverters, and the second pair of transistors is coupled between an output of the third inverter in the odd number of series connected inverters and an output of the first inverter in the odd number of series connected inverters.

46. The memory device of claim 30, further comprising an electrical component loading the output of the first of the inverters in the odd numbered series and in the even numbered series, the electrical component being unconnected to any other portion of the phase splitter.

47. The memory device of claim 46, wherein each of the electrical component comprises a respective inverter.

48. The memory device of claim 30 wherein the transistors in the first and second pairs comprise diode-coupled transistors.

49. A memory device, comprising:

an array of memory cells;

an address decoder adapted to receive an address and to specify a location in the array of memory cells corresponding thereto;

a read/write circuit coupling data to and from the specified location in the array of memory cells;

a control logic circuit receiving command signals and generating control signals corresponding thereto; and

a phase splitter coupled to the control logic circuit, the phase splitter being operable to receive an input clock signal and to apply first and second complimentary output clock signals corresponding thereto, the phase splitter comprising:

an even number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the first output clock signal;

an odd number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the second output clock signal; and

an inverter having an input coupled between an output of an inverter that is an odd number of inverters from the input clock signal and an output of an inverter that is an even number of inverters from the input clock signal.

50. The memory device of claim 49 further comprising an inverter coupled between an output of an inverter that is N number of inverters from the input clock signal and an output of an inverter that is N+1 number of inverters from the input clock signal, where N comprises a positive integer.

51. The memory device of claim 50 wherein N comprises an even positive integer.

52. The memory device of claim 49 wherein the even number of series connected inverters comprises 2 inverters and the odd number of series connected inverters comprises 3 inverters.

53. The memory device of claim 52 wherein the inverter has an input coupled to an output of the second inverter in the odd number of series connected inverters and an output coupled to an output of the first inverter in the even number of series connected inverters.

54. The memory device of claim 49 wherein the even number of series connected inverters comprises 2 inverters and the odd number of series connected inverters comprises 5 inverters.

55. The memory device of claim 49, further comprising an electrical component loading the output of the first of the inverters in the odd numbered series and in the even numbered series, the electrical component being unconnected to any other portion of the phase splitter.

56. The memory device of claim 55, wherein each of the electrical component comprises a respective inverter.

57. A memory device, comprising:

an array of memory cells;

an address decoder adapted to receive an address and to specify a location in the array of memory cells corresponding thereto;

a read/write circuit coupling data to and from the specified location in the array of memory cells;

a control logic circuit receiving command signals and generating control signals corresponding thereto; and

a phase splitter coupled to the control logic circuit, the phase splitter being operable to receive an input clock signal and to apply first and second complimentary output clock signals corresponding thereto, the phase splitter comprising:

an even number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the first output clock signal;

an odd number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the second output clock signal; and

an electrical component loading the output of the first of the inverters in the odd series numbered and in the even numbered series, the electrical component being unconnected to any other portion of the phase splitter.

58. The memory device of claim 57, wherein each of the electrical component comprises a respective inverter.

59. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a memory device coupled to the processor through the processor bus, the memory device comprising:

an array of memory cells;

an address decoder adapted to receive an address and to specify a location in the array of memory cells corresponding thereto;

a read/write circuit coupling data to and from the specified location in the array of memory cells;

a control logic circuit receiving command signals and generating control signals corresponding thereto; and

a phase splitter coupled to the control logic circuit, the phase splitter being operable to receive an input clock signal and to apply first and second complimentary output clock signals corresponding thereto, the phase splitter comprising:

an even number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the first output clock signal;

an odd number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the second output clock signal;

a first pair of transistors each of which is coupled between an output of one of the inverters in the even number of series connected inverters and respective first and second nodes; and

a second pair of number of series connected inverters transistors each of which is coupled between an output of one of the inverters in the odd number of series connected inverters and respective third and fourth nodes.

60. The computer system of claim 59 further comprising an inverter coupled between an output of an inverter in the even number of series connected inverters that is N number of inverters from the input clock signal and an output of an inverter in the odd number of series connected inverters that is N+1 number of inverters from the input clock signal, where N comprises a positive integer.

61. The computer system of claim 60 wherein N comprises an odd positive integer.

62. The computer system of claim 59 wherein at least one transistor in each pair has a gate that is coupled to one of the first and second voltages.

63. The computer system of claim 62 wherein the transistors in each pair has a respective gate that is coupled to the first and second voltages, respectively.

64. The computer system of claim 59 wherein the first and second nodes comprises a common node.

66. The computer system of claim 64 wherein the first, second, third and fourth nodes comprises a common node.

66. The computer system of claim 65 wherein the common node comprises an output of one of the inverters that is an odd number of inverters from the input clock signal, and the inverter in each of the having an output to which the respective first and second pairs of transistors are coupled comprise an odd number of inverters from the input clock signal.

67. The computer system of claim 59 wherein the transistor in each pair have a gate that is coupled to one of the inverters in one of the series of inverters.

68. The computer system of claim 67 wherein a first transistor in each pair is has a drain that is coupled to a supply voltage, and a second transistor in each pair is coupled to ground potential.

69. The computer system of claim 59 wherein the third and fourth nodes comprises a common node.

70. The computer system of claim 59 wherein the even number of series connected inverters comprises two inverters and the odd number of series connected inverters comprises three inverters.

71. The computer system of claim 70 wherein the first pair of transistors is coupled between an output of the third inverter in the odd number of series connected inverters and an output of the first inverter in the even number of series connected inverters, and the second pair of transistors is coupled between an output of the third inverter in the odd number of series connected inverters and an output of the first inverter in the odd number of series connected inverters.

72 The computer system of claim 71 wherein the even number of series connected inverters comprises 2 inverters and the odd number of series connected inverters comprises five inverters.

73. The computer system of claim 72 wherein the first pair of transistors is coupled between an output of the fifth inverter in the odd number of series connected inverters and an output of the first inverter in the even number of series connected inverters, and the second pair of transistors is coupled between an output of the third inverter in the odd number of series connected inverters and an output of the first inverter in the odd number of series connected inverters.

74. The computer system of claim 59 wherein the first and third nodes comprise a supply voltage, and the second and fourth nodes comprises a ground potential.

75. The memory device of claim 59 wherein the transistors in the first and second pairs comprise diode-coupled transistors.

76. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a memory device coupled to the processor through the processor bus, the memory device comprising:

an array of memory cells;

an address decoder adapted to receive an address and to specify a location in the array of memory cells corresponding thereto;

a read/write circuit coupling data to and from the specified location in the array of memory cells;

a control logic circuit receiving command signals and generating control signals corresponding thereto; and

a phase splitter coupled to the control logic circuit, the phase splitter being operable to receive an input clock signal and to apply first and second complimentary output clock signals corresponding thereto, the phase splitter comprising:

an even number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the first output clock signal;

an odd number of series connected inverters, the first of the inverters in the series coupled to receive the input clock signal and the last of the inverters in the series generating the second output clock signal; and

an inverter being coupled between an output of an inverter that is an odd number of inverters from the input clock signal and an output of an inverter that is an even number of inverters from the input clock signal.

77. The computer system of claim 76 further comprising an inverter coupled between an output of an inverter that is N number of inverters from the input clock

signal and an output of an inverter that is N+1 number of inverters from the input clock signal, where N comprises a positive integer.

78. The computer system of claim 77 wherein N comprises an odd positive integer.

79. The computer system of claim 76 wherein the even number of series connected inverters comprises 2 inverters and the odd number of series connected inverters comprises 3 inverters.

80. The computer system of claim 79 wherein the inverter has an input coupled to an output of the second inverter in the odd number of series connected inverters, and an output coupled to an output of the first inverter in the even number of series connected inverters.

81. The computer system of claim 76 wherein the even number of series connected inverters comprises 2 inverters and the odd number of series connected inverters comprises 5 inverters.

82. A method of generating first and second complimentary output clock signal from an input clock signal, comprising:

generating the first output clock signal by coupling the input clock signal through a first branch containing an odd number of inverters;

generating the second output clock signal by coupling the input clock signal through a second branch containing an even number of inverters; and

coupling an output of an inverter in one of the branches to an input of an inverter in the other of the branches.

83. The method of claim 82, further comprising:

coupling an output from a first inverter in the first branch to a first logic level when the output of the inverter is at a second logic level, and coupling the output from the first inverter in the first branch to the second logic level when the output of the inverter is at the first logic level, the output being coupled through a circuit component that compensates for process variations in the first inverter; and

coupling an output from a second inverter in the second branch to the first logic level when the output of the inverter is at the second logic level, and coupling the output from the second inverter in the second branch to a second logic level when the output of the inverter is at the first logic level, the output being coupled through a circuit component that compensates for process variations in the second inverter.

84. The method of claim 82 wherein the act of coupling an output of an inverter in one of the branches to an input of an inverter in the other of the branches comprises:

inverting the output of an inverter in one of the branches located N inverters from the input clock signal; and

coupling the inverted output to an inverter in the other of the branches located N+1 inverters from the input clock signal.

85. A method of generating first and second complimentary output clock signal from an input clock signal, comprising:

generating the first output clock signal by coupling the input clock signal through a first branch containing an odd number of inverters;

generating the second output clock signal by coupling the input clock signal through a second branch containing an even number of inverters;

coupling an output from a first inverter in the first branch to a first logic level when the output of the inverter is at a second logic level, and coupling the output from the first inverter in the first branch to the second logic level when the output of the inverter is at the first logic level, the output being coupled through a circuit component that compensates for process variations in the first inverter; and

coupling an output from a second inverter in the second branch to the first logic level when the output of the inverter is at the second logic level, and coupling the output from the second inverter in the second branch to a second logic level when the output of the inverter is at the first logic level, the output being coupled through a circuit component that compensates for process variations in the second inverter.

86. The method of claim 85 wherein the acts of coupling the outputs of the first and second inverters to first and second logic levels comprise coupling the outputs of the first and second inverters through diode-coupled MOSFET transistors.

87. The method of claim 86 wherein the acts of coupling the outputs of the first and second inverters through diode-coupled MOSFET transistors comprise coupling the outputs to ground potential through respective diode-coupled PMOS transistors and coupling the outputs to a supply voltage through respective diode-coupled NMOS transistors.

88. A method of scaling a circuit having at least a first logic component driving a second logic component, the method comprising:

downwardly scaling the first logic component;

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downwardly scaling the second logic component to a greater extent than the scaling of the first logic component so that the second logic component is scaled to a greater extent than the first logic component; and

coupling an electrical loading component to the output of the first logic component, the electrical component being unconnected to any other portion of the circuit, the electrical loading component maintining the timing relat.

89. The method of claim 88, wherein each of the first and second logic components comprises a respective inverter, and wherein each of the electrical components comprises a respective inverter.

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